N-Ch 100V Fast Switching MOSFETs

Features

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

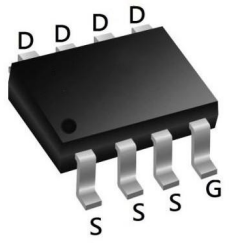
Product Summary

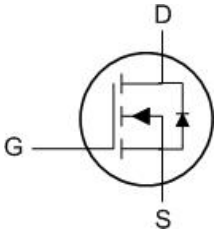
BVDSS	RDSON	ID
100V	61mΩ	15A

Applications

- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

SOP8 Pin Configuration





Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ 10V[1,6]	15	A
I_D@T_C=100℃	Continuous Drain Current, V_{GS} @ 10V[1,6]	10.7	A
I_{DM}	Pulsed Drain Current[2]	80	A
EAS	Single Pulse Avalanche Energy[3]	22	mJ
I_{AS}	Avalanche Current	---	A
P_D@T_C=25℃	Total Power Dissipation[4]	46	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1]	---	---	℃/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	---	2.7	℃/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	100	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BV_{DSS} Temperature Coefficient	Reference to 25℃ , I_D=1mA	---	---	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V , I_D=5A	---	61	75	mΩ
		V_{GS}=4.5V , I_D=4A	---	77	100	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =250uA	1.3	1.8	2.3	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	---	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=100V , V_{GS}=0V , T_J=25℃	---	---	1	uA
		V_{DS}=100V, V_{GS}=0V , T_J=100℃	---	---	100	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=10V , I_D=5A	---	---	---	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	---	---	Ω
Q_g	Total Gate Charge	V_{DS}=50V , V_{GS}=10V , I_D=10A	---	3.7	---	nC
Q_{gs}	Gate-Source Charge		---	0.8	---	
Q_{gd}	Gate-Drain Charge		---	1	---	
$T_{d(on)}$	Turn-On Delay Time	VGS=10V, VDD=50V, RG=3Ω, ID=10A	---	8	---	ns
T_r	Rise Time		---	16	---	
$T_{d(off)}$	Turn-Off Delay Time		---	17	---	
T_f	Fall Time		---	14	---	
C_{iss}	Input Capacitance	V_{DS}=50V , V_{GS}=0V , f=1MHz	---	228	---	pF
C_{oss}	Output Capacitance		---	58	---	
C_{rss}	Reverse Transfer Capacitance		---	1.9	---	

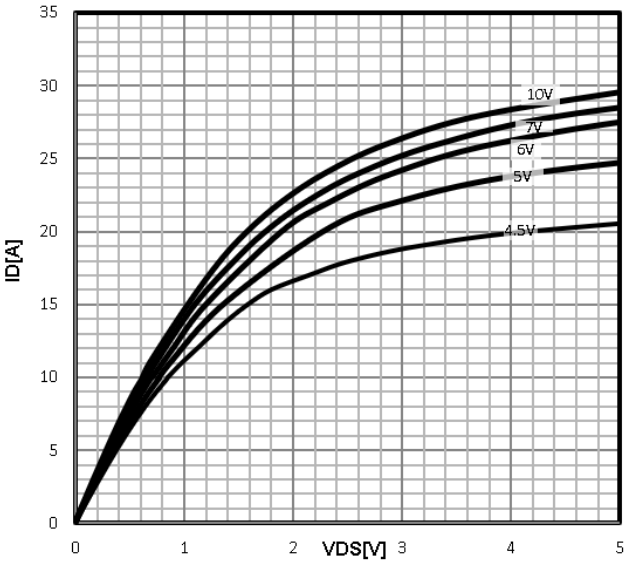
Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current[1,4]	V_G=V_D=0V , Force Current	---	---	15	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=20A , T_J=25℃	---	---	1.2	V
t_{rr}	Reverse Recovery Time	IF=10A , di/dt=100A/μs , T_J=25℃	---	22	---	nS
Q_{rr}	Reverse Recovery Charge		---	18	---	nC

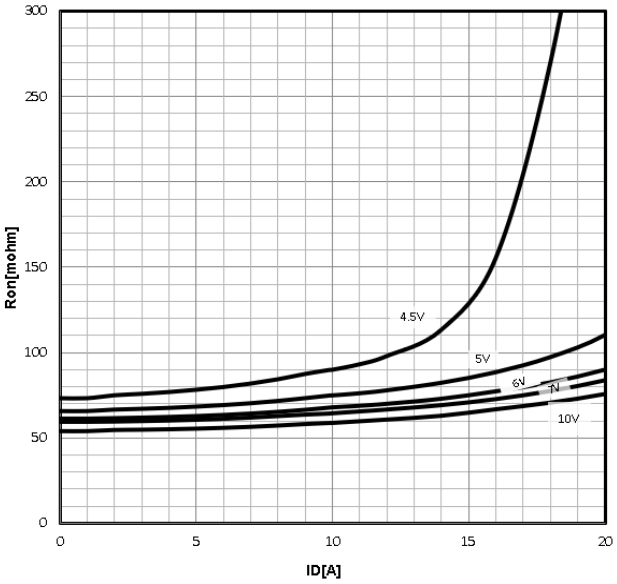
Note :
1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
3.The EAS data shows Max. rating . The test condition is TJ = 25℃,VDD=50V,VGS=10V,L=5mH.
4.The power dissipation is limited by 150℃ junction temperature
5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Characteristics Curve:

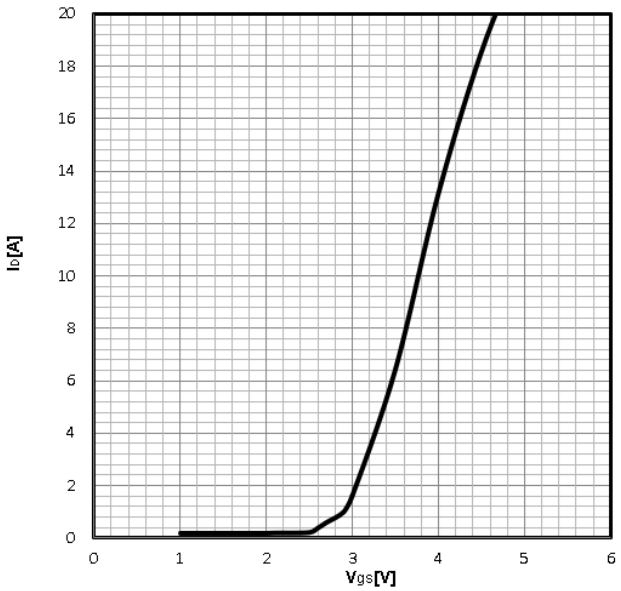
Typ. output characteristics
$I_D=f(V_{DS})$



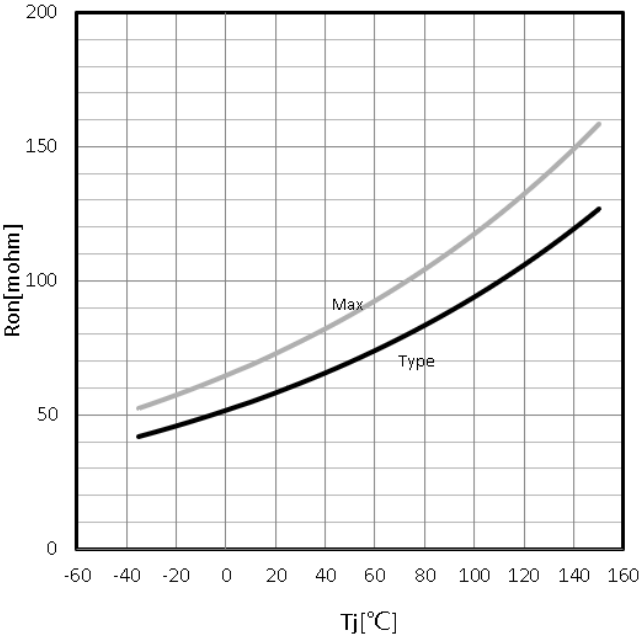
Typ. drain-source on resistance
$R_{DS(on)}=f(I_D)$



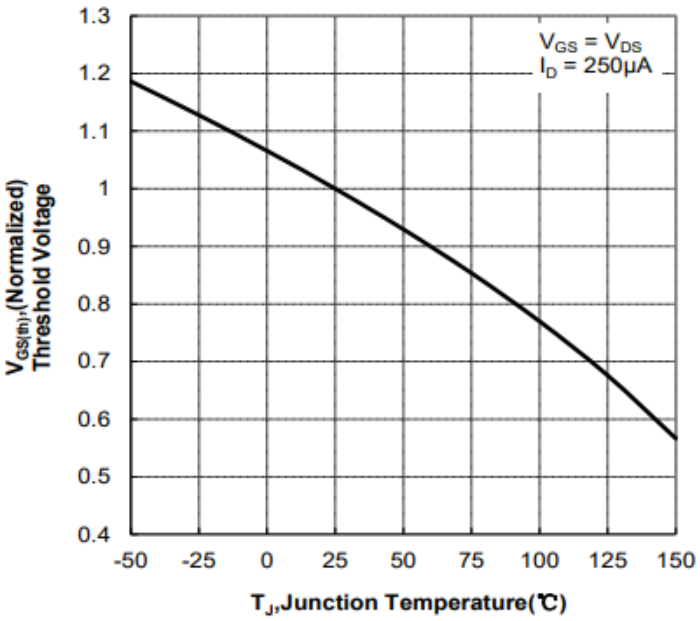
Typ. transfer characteristics
$I_D=f(V_{GS})$



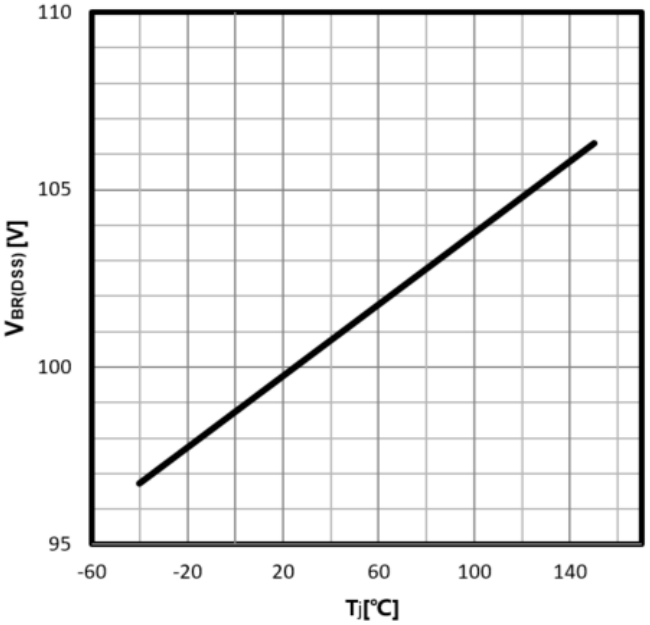
Drain-source on-state resistance
$R_{DS(on)}=f(T_j);I_D=5A;\ V_{GS}=10V$



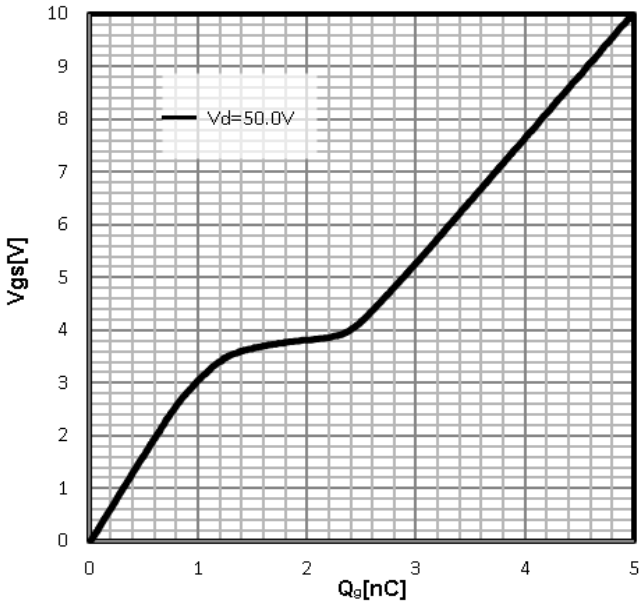
Gate Threshold Voltage
$V_{TH}=f(T_j)$; I_D=250uA



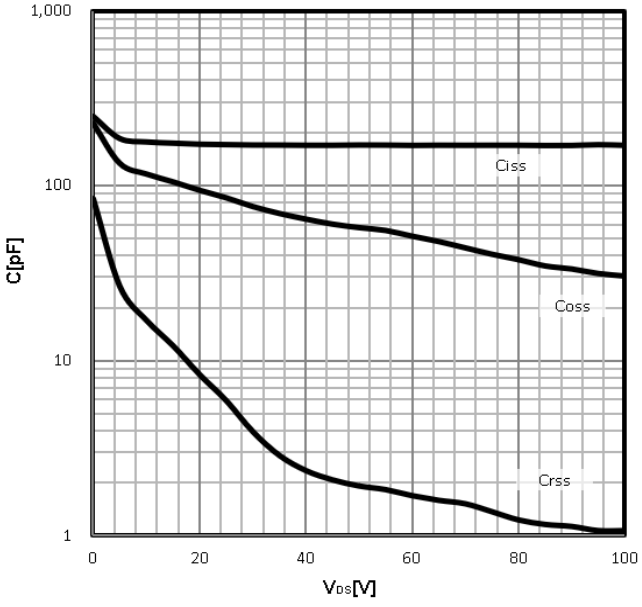
Drain-source breakdown voltage
$V_{BR(DSS)}=f(T_j)$; I_D=250uA



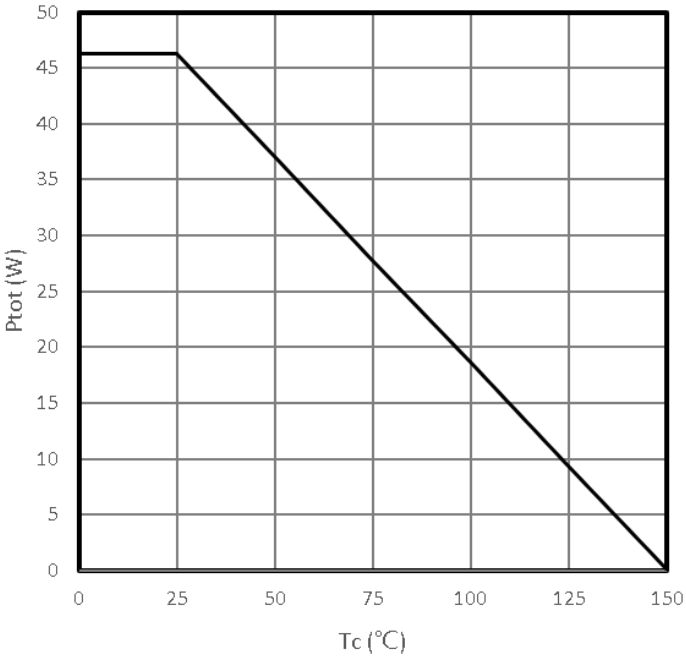
Typ. gate charge
$V_{GS}=f(Q_g)$; I_D=10A



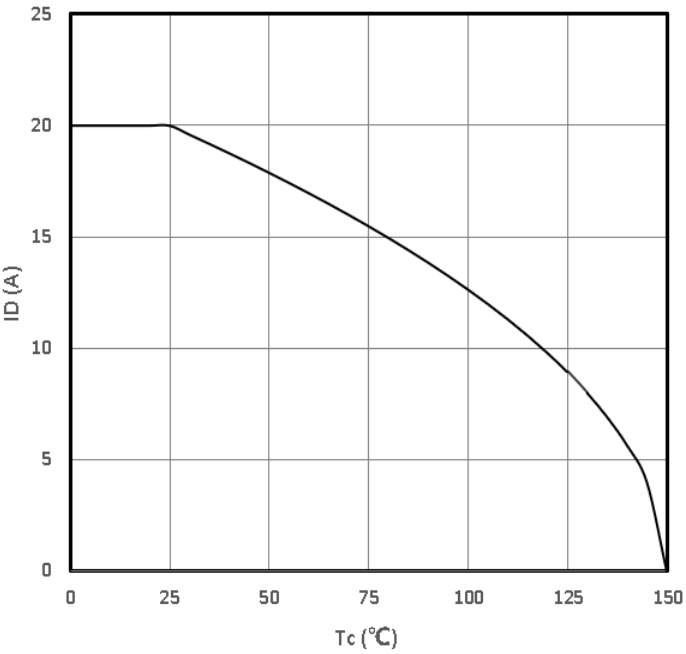
Typ. capacitances
C =f(V_{DS}); V_{GS}=0V; f =1MHz



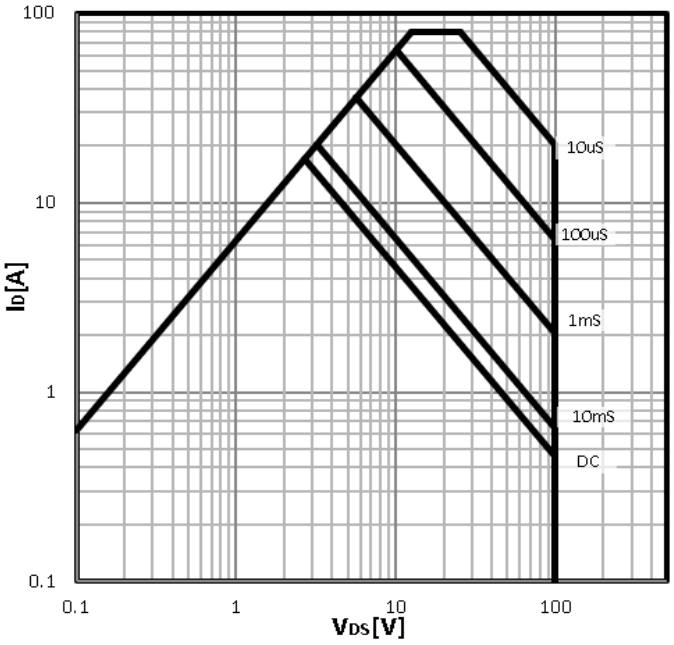
Power Dissipation
$P_{tot}=f(T_C)$



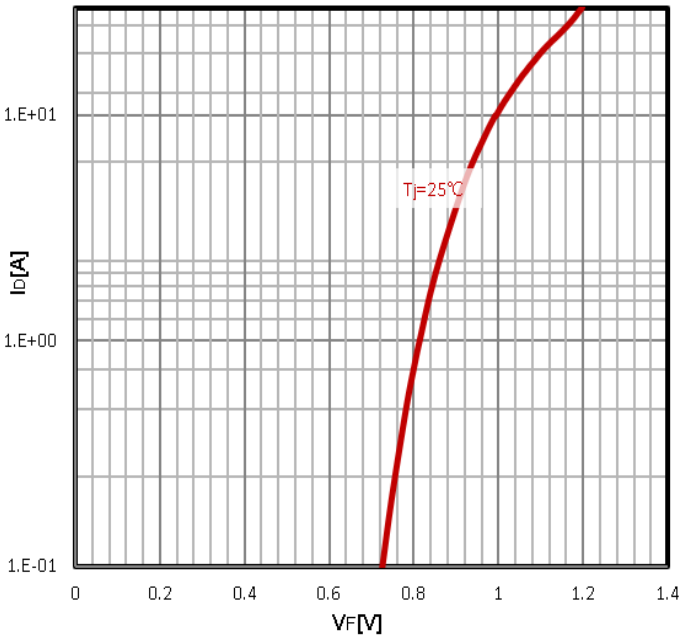
Maximum Drain Current $I_D=f(T_C)$



Safe operating area
$I_D=f(V_{DS})$

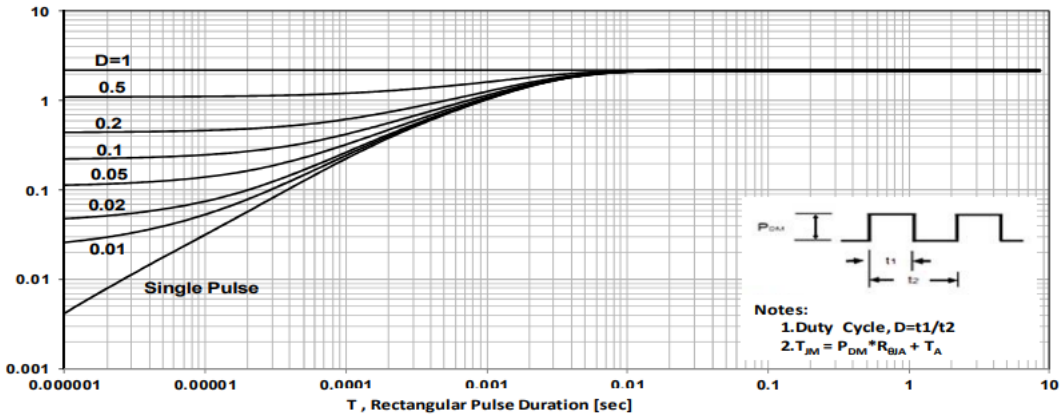


Body Diode Forward Voltage Variation
$I_F=f(V_{GS})$

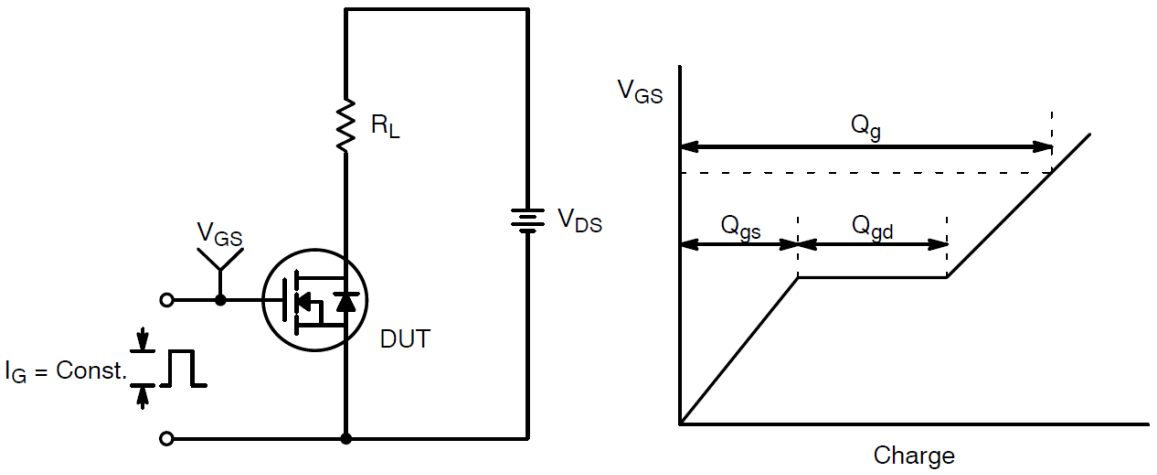


Max. transient thermal impedance

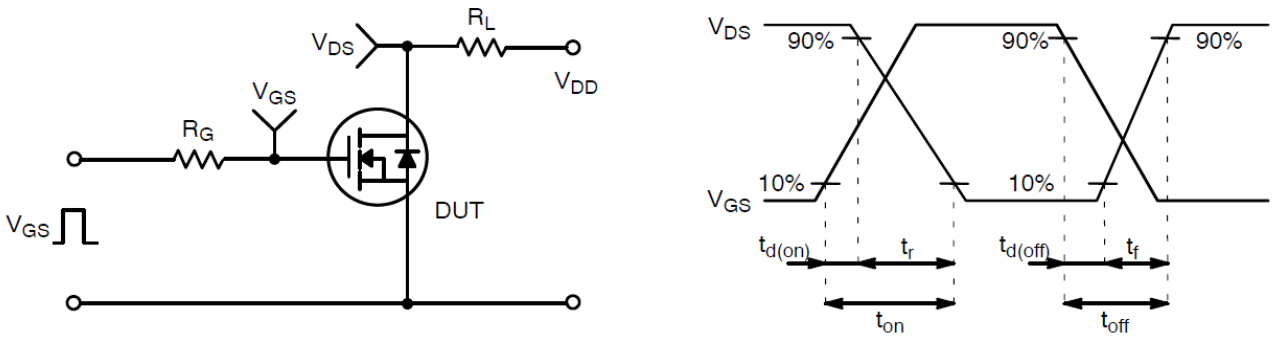
$Z_{thJC}=f(t_p)$



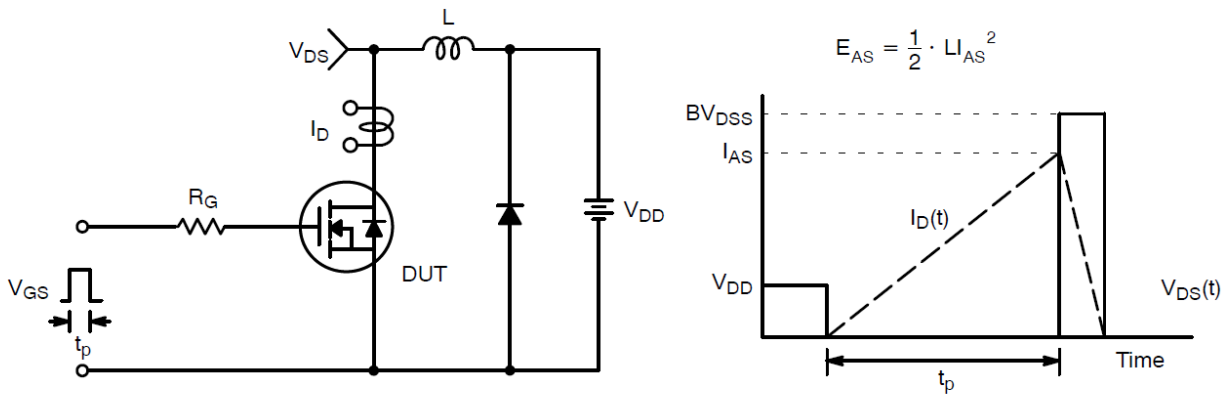
Test Circuit and Waveform:



Gate Charge Test Circuit & Waveform

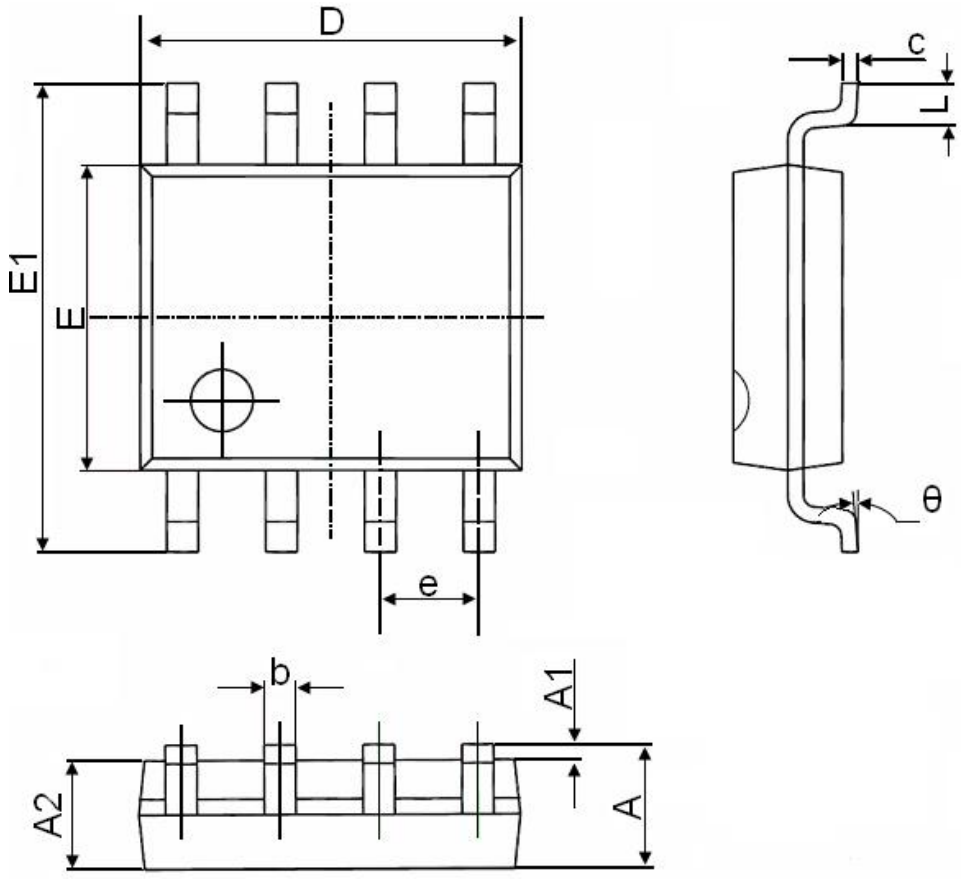


Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

SOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°